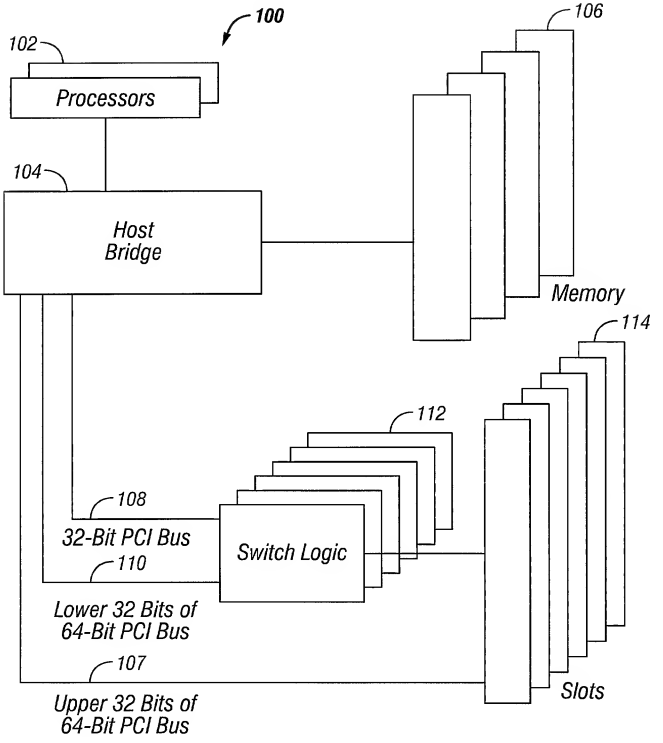

FIG. 1

Patent Application

PATENT 08066801

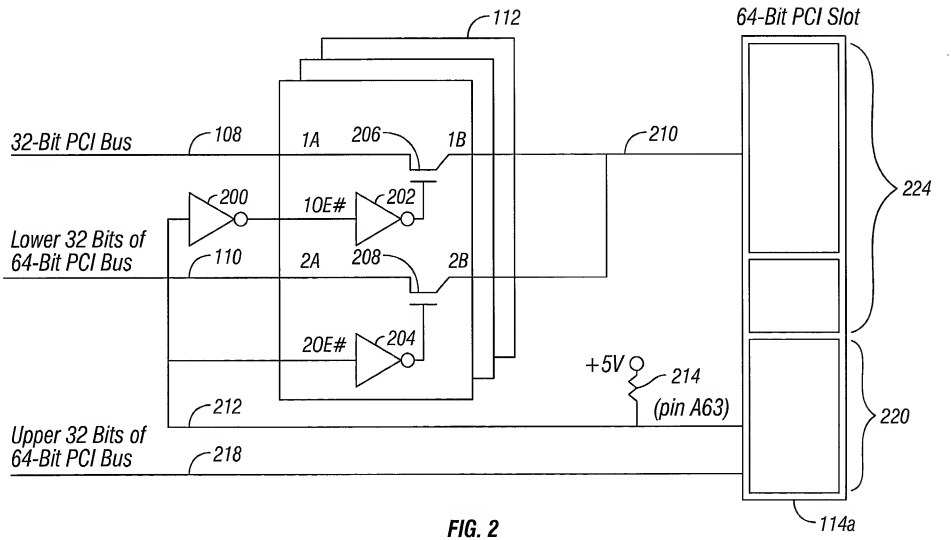

FIG. 2

300

Inputs		Inputs/Outputs	
1OE#	2OE#	1A, 1B	2A, 2B
L	L	1A=1B	2A=2B
L	H	1A=1B	Z
H	L	Z	2A=2B
H	H	Z	Z

FIG. 3

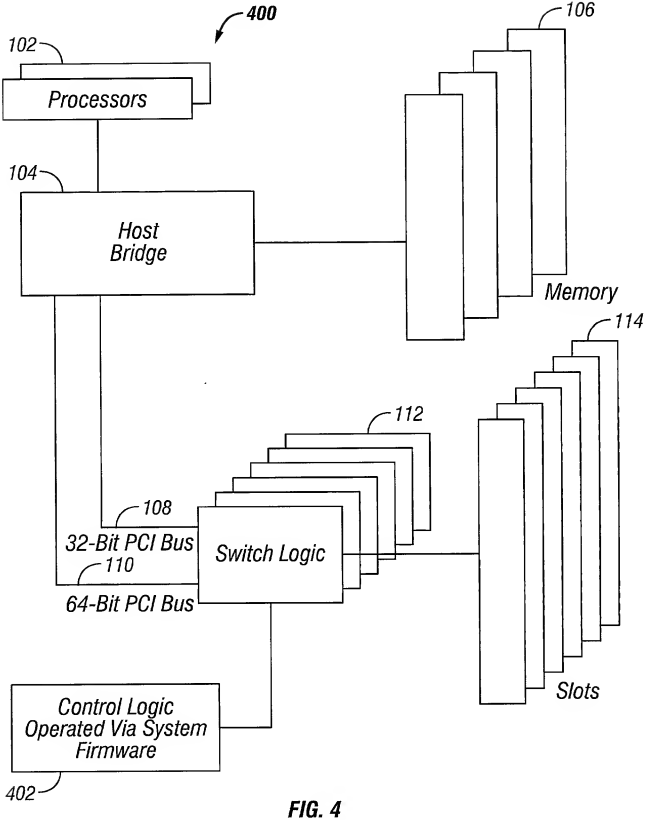
400
102
Processors
104
Host Bridge
106
Memory
114
112
108
32-Bit PCI Bus
110
64-Bit PCI Bus
Switch Logic
Slots
Control Logic Operated Via System Firmware
402

FIG. 4

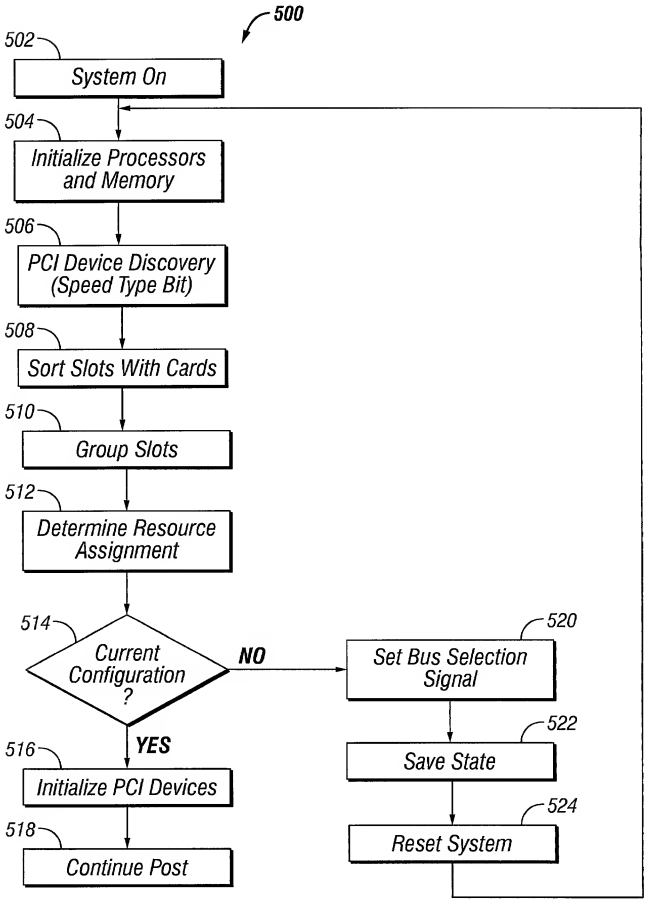
500
502
System On
504
Initialize Processors and Memory
506
PCI Device Discovery (Speed Type Bit)
508
Sort Slots With Cards
510
Group Slots
512
Determine Resource Assignment
514
Current Configuration ?
NO
520
Set Bus Selection Signal
522
Save State
524
Reset System
YES
516
Initialize PCI Devices
518
Continue Post

FIG. 5

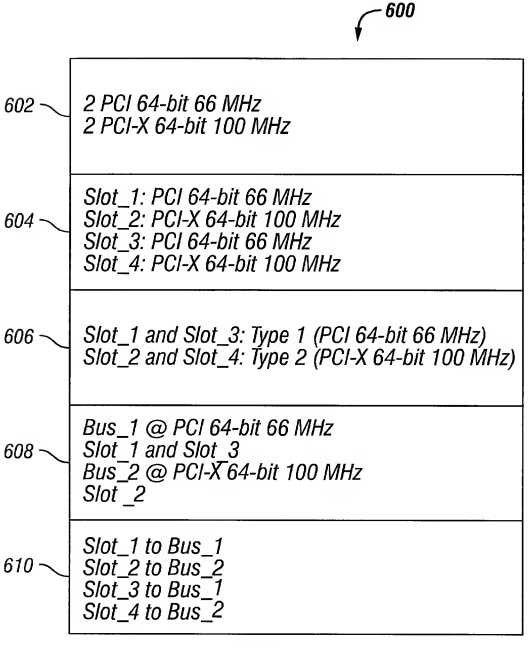
600
602
2 PCI 64-bit 66 MHz
2 PCI-X 64-bit 100 MHz
604
Slot_1: PCI 64-bit 66 MHz
Slot_2: PCI-X 64-bit 100 MHz
Slot_3: PCI 64-bit 66 MHz
Slot_4: PCI-X 64-bit 100 MHz
606
Slot_1 and Slot_3: Type 1 (PCI 64-bit 66 MHz)
Slot_2 and Slot_4: Type 2 (PCI-X 64-bit 100 MHz)
608
Bus_1 @ PCI 64-bit 66 MHz
Slot_1 and Slot_3
Bus_2 @ PCI-X 64-bit 100 MHz
Slot _2
610
Slot_1 to Bus_1
Slot_2 to Bus_2
Slot_3 to Bus_1
Slot_4 to Bus_2

FIG. 6

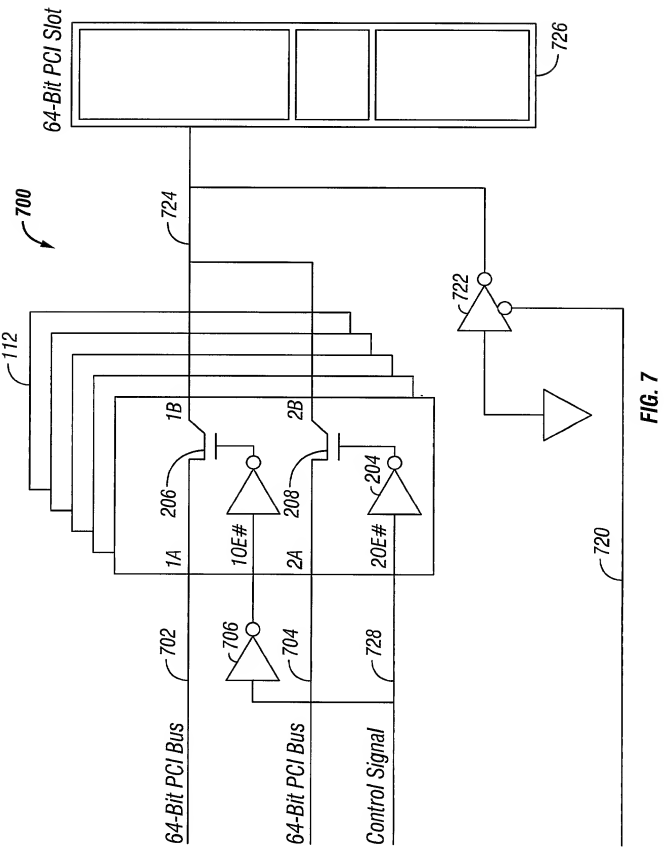
700
112
64-Bit PCI Slot
726
724
722
1B
2B
206
208
204
1A
10E#
2A
20E#
706
702
704
728
720
64-Bit PCI Bus
64-Bit PCI Bus
Control Signal

FIG. 7

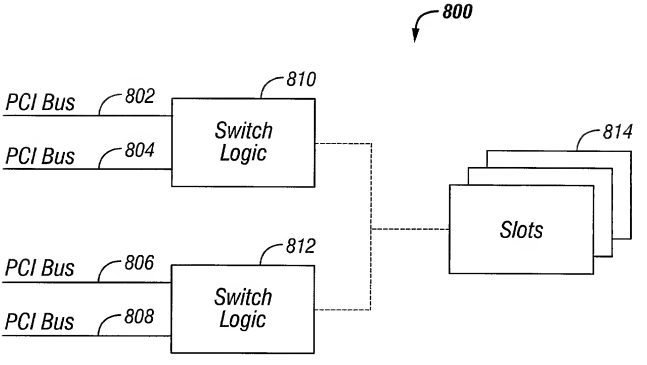
800
PCI Bus
802
PCI Bus
804
Switch Logic
810
814
Slots
PCI Bus
806
PCI Bus
808
Switch Logic
812

FIG. 8

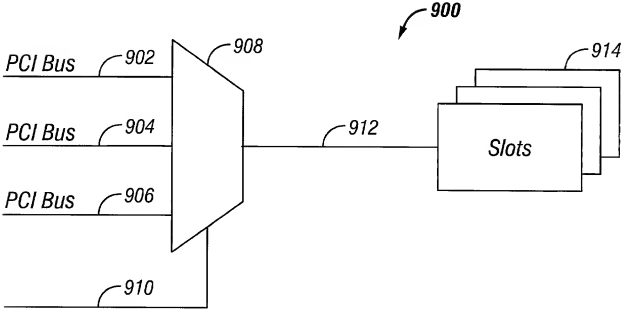
900
PCI Bus
902
PCI Bus
904
PCI Bus
906
908
912
914
Slots
910

FIG. 9